IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	Saulsbury et al.		
App. No.:	09/992,064	Conf. No.:	4869
Filed:	November 21, 2001	Art Unit:	2193
Title:	METHODS AND APPARATUS FOR PERFORMING PIXEL AVERAGE OPERATIONS	Examiner:	Do, Chat C.

REPLY BRIEF

MAIL STOP REPLY BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant (hereafter "Appellant") hereby submits this Reply Brief in response to the Examiner's Answer mailed September 18, 2007.

Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences (hereafter the "Board") based on this Reply Brief and the previously submitted Appeal Brief.

I. SUMMARY OF THE CLAIMED SUBJECT MATTER

The Examiner's Answer indicates that the summary of claimed subject matter in the Appeal Brief is deficient. Although the Appellant respectfully disagrees, the following provides a more verbatim mapping of the language used in the independent claims.

Claims 1 and 8 recite "decoding a single machine code instruction comprising an address for a first input register, an address for a second input register, an address for an output register, an op code indicating a function to perform, and a rounding factor." For example, as illustrated in Figure 4, a pixel averaging sub-instruction 404 may comprise an address 416 for a first input register, an address 420 for a second input register, an address 424 for an output register, an op code 412 indicating a function to perform, and a rounding factor r. *See specification, page 8, lines 17-21, 25-26 and 29-30.* Instruction decode and issue logic 58 decodes the sub-instructions. *See specification, page 6, lines 14-16 and Figure 2.*

Claim 1 further recites "loading a plurality of first operands from the first input register" and "loading a plurality of second operands from the second input register." Claim 8 similarly recites "loading a first operand from an A1 field of the first input register" and "loading a second operand from a B1 field of the second input register." As described with respect to Figure 5, an instruction processor 500, coupled to first and second input registers 508-1, 508-2 loads the input operands from the input registers 508. *See specification, page 9, lines 11-12 and Figure 5.* As described with respect to Figure 6, an instruction processor 500 reads first and second input operands 512, 516 from the respective registers 508-1, 508-2, which each have a plurality of fields (e.g., 512-1 to 512-4 and 516-1 to 516-4)). *See specification, page 9, lines 24-30 and Figure 6.*

Claim 1 recites "producing an average, based on the op code, of one of the plurality of first operands and one of the plurality of second operands producing an average, based on the op code, of the first operand and the second operand" and "storing the average in the output register." Claim 8 similarly recites "producing an average, based on the op code, of the first operand and the second operand" and "storing the average in a C1 filed of the output register." The instruction processor 500 performs the pixel average function and stores the results in the output register 504." *See specification, page 9, lines 13 and 31, and Figures 5 an 6.*

Claims 1 and 8 recite "wherein the rounding factor indicates which of a plurality of rounding algorithms to use in producing the average, the plurality of rounding algorithms comprising: a first rounding algorithm able to produce a change in the average; and a second rounding algorithm able to produce a change in the average." The rounding factor r indicates

the way to round the average before storage in the output register. *See specification, page 8, lines 29-31.* The rounding factor serves to round the pixel average in either of two different ways depending on the pixel averaging algorithm desired by the user. *See specification, page 10, lines 8-9.*

In combination with the summary of claimed subject matter in the Appeal Brief, the Appellant respectfully submits that the individual limitations of claims 1 and 8 are addressed in sufficient detail.

Independent claim 18 recites "a first input register comprising a plurality of first fields," "a second input register comprising a plurality of second fields," and "a rounding factor indicated by a single machine code instruction." These features are described, for example, as first register 508-1 including fields 512-1 to 512-4, second register 508-2 including fields 516-1 to 516-4, and rounding factor 604. *See specification page 9, lines 22-33, and Figure 6.*

Claim 18 recites "a plurality of average modules respectively coupled to the first and second fields, the modules configured to perform an averaging function indicated by an op code in the single machine code instruction." These features are described, for example, as average modules 600-1 to 600-4, which perform the function indicated by the op code. *See specification page 10, lines 1-7, Figures 6 and 7, and specification page 8, lines 15-16.*

Claim 18 also recites "an output register comprising a plurality of third fields, wherein: the third fields are respectively coupled to the plurality of average modules." These features are illustrated by an output register 504 with a plurality fields 524-1 to 524-4, which are respectively coupled to the average modules 600-1 to 600-4. *See specification page 9, lines 22-33 and Figure 6.*

Claim 18 further recites that "the rounding factor affects how the plurality of average modules round results to produce an average," "the rounding factor indicates which of a plurality of rounding algorithms to use in producing the average," and "the plurality of rounding algorithms comprising: a first rounding algorithm able to produce a change in the average; and a second rounding algorithm able to produce a change in the average. As discussed above with respect to claims 1 and 8, the rounding factor indicates the way to round the average (*specification, page 8, lines 29-31)* and serves to round the pixel average in either of two different ways (*specification, page 10, lines 8-9*), thus affecting how the plurality of modules round results.

As also discussed above with respect to claims 1 and 8, "the single machine code instruction comprises an address for the first input register, an address for the second input register, an address for the output register, the op code, and the rounding factor" is described,

for example, as a pixel averaging sub-instruction 404 comprising an address 416 for a first input register, an address 420 for a second input register, an address 424 for an output register, an op code 412 indicating a function to perform, and a rounding factor r. *See specification, page 8, lines 17-21, 25-26 and 29-30, and Figure 4.*

In combination with the summary of claimed subject matter in the Appeal Brief, the Appellant respectfully submits that the individual limitations of claim 18 are also addressed in sufficient detail.

II. REBUTTAL OF EXAMINER'S RESPONSE TO ARGUMENTS

A. Independent claims 1 and 8

The Appellant does argue that none of the text cited by the final Office action supports the conclusion that Sijstermans discloses a single machine code instruction including the identified registers, op code and rounding factor. However, the critical point is that that Sijstermans simply fails to disclose that the rounding factor is included in the same instruction.

The Examiner's reliance on column 2, lines 31-49, column 3, lines 45-55, and column 12, lines 45-57, is misplaced.

Column 2, lines 31-49, of Sijstermans does not support the Examiner's position that the rounding factor is included in the same instruction. On the contrary, this text discloses that "a single machine instruction can be used to select one of a variety of rounding modes" and that "[o]nce the rounding mode is set, the programmable processor uses the mode when executing subsequent machine instructions that perform arithmetic operations." (emphasis added) In other words, Sijstermans teaches that one machine instruction sets the rounding mode and that other different machine instructions are executed to perform arithmetic operations, with the rounding mode already set. Thus, the rounding mode is not included in the subsequent machine instructions because it is not needed with the rounding mode already set.

Column 3, lines 45-55, of Sijstermans also does not support the Examiner's position that the rounding factor is included in the same instruction. On the contrary, this text discloses that the instruction to be decoded is fetched from an instruction stream, while the rounding mode is specified by the control register. As such, the rounding mode is clearly not included in the instruction to be decoded, otherwise it would not need to be specified by the control register.

Column 12, lines 45-57, of Sijstermans also does not support the Examiner's position that the rounding factor is included in the same instruction. On the contrary, this text discloses that the type of rounding applied depends on the value of an integer rounding mode value, as shown in Table 1. This text does not indicate that the integer rounding mode value is included in the instruction. Instead, this text refers to Table 1 and not any instruction containing the value.

In fact, none of the cited text states that the rounding mode or the rounding mode value is included in the same instruction as the register addresses and the op code. As discussed above, Sijstermans teaches that the rounding mode is set for one or more instructions performing arithmetic operations by a different instruction and that the rounding mode as set is

found in the control register 22, not in the instructions performing arithmetic operations. The citations provided in the Examiner's answer thus do not remedy the lack of any factual support in Sijstermans for the Examiner's position.

The Appellant notes that the Examiner's response to arguments does not specifically address the paragraph bridging pages 7 and 8 of the Appeal Brief. Thus, the Appellant respectfully resubmits that the VLIW approach does not inherently package all instructions and that neither the final Office action nor the Examiner's response to arguments establishes that the VLIW utilized in Sijstermans includes the rounding factor.

The Appellant further notes that the Examiner's response to arguments does not address the second paragraph on page 8 of the Appeal Brief, although the Examiner's response to arguments purports to. With respect to this paragraph, the Examiner's response to arguments only provides a definition of a VLIW. This does not rebut the Appellant's argument that the various instructions, such as "[if regard]avg4_bu rsrc1 rsrc2 rsrc3 rsrc4 rdest" cited by the final Office Action, processed by a VLIW processor do not include or identify a rounding factor.

As the final Office action fails to identify any code corresponding to the rounding factor in the cited VLIW instruction, and the Examiner's answer fails to rebut the Appellants argument in this regard, the Appellant understands that this basis set forth in the final Office action is no longer considered valid and should be disregarded. In other words, the failure of the Examiner's Answer to provide any rebuttal of the argument that none of the operational instructions disclosed by Sijstermans includes the rounding factor should be considered an admission that no VLIW in Sijstermans includes the rounding factor.

The Appellant notes that the Examiner's response to arguments also does not specifically address the third paragraph on page 8 of the Appeal Brief. Thus, the Appellant respectfully resubmits that Sijstermans specifically teaches that the rounding factor is set by a separate instruction, not by the VLIW.

Finally, the Appellant notes that the Examiner's response to arguments provided in paragraph 12 on page 12 of the Examiner's Answer does not particularly address the Appellant's arguments in the paragraph bridging pages 8 and 9 of the Appeal Brief, and further presents a legally flawed position. The Examiner's response to arguments in this regard only restates the definition of a VLIW and does not deal with the probative value of the claims of Sijstermans in this case. No rebuttal to the fact that each and every claim of Sijstermans

specifically recites two separate instructions is provided. As the claims are part of the disclosure of Sijstermans, the Appellant respectfully submits that it is improper to disregard the Appellant's argument that this portion of the disclosure of Sijstermans specifically teaches away from decoding a single machine code instruction as recited in Appellant's claims 1 and 8.

Although a VLIW may be "capable" of including both instructions, it would be improper to modify Sijstermans contrary to its teachings because doing so would change its principle of operation. This would violate MPEP § 2143.02(VI). As discussed above, Sijstermans' approach is to have the rounding mode set by a user in a separate instruction. The proposed modification would defeat this purpose and would render Sijstermans unsatisfactory for this intended purpose. This would violate MPEP § 2143.02(V).

B. Independent claim 18

In response to the Appellant's arguments in the paragraph bridging pages 8 and 9 of the Appeal Brief, the Examiner's Answer cites Figure 3 of Sijstermans as disclosing a plurality of averaging modules to perform an averaging function. As Figure 3 of Sijstermans is a flow diagram, the Appellant fails to understand how it may be considered to disclose structure.

The description of Figure 3 in Sijstermans (column 5, line 66 – column 6, line 38) makes no mention of a plurality of averaging modules or corresponding structure, and the Examiner's Answer fails to indicate any specific structure that is alleged to be a plurality of averaging modules, a deficiency of the final Office action argued in the Appeal Brief. Column 6, lines 25-45, cited in the Examiner's response to arguments does not disclose any structure that could arguably correspond to the plurality of averaging modules recited in claim 18.

The Appellant notes that the allegation that the process of averaging four vectors "implicitly" or "inherently" involves a plurality of averaging modules is presented for the first time in the Examiner's Answer. The Appellant respectfully submits that a factual basis or technical reasoning should be required, rather than the unsupported conclusion that the operation described in column 6, lines 25-45, of Sijstermans involves a plurality of averaging modules.

The Appellant respectfully resubmits that a proper basis for rejection of apparatus claim 18 cannot be made without addressing the specific structures recited therein. The rejection of claim 18 by asserting that claim 18 "is an apparatus claim of claim 1" fails to address the specific structures recited in claim 18. The similarity of the claim 18 to claim 1 is insufficient to "apply the same rationale" because no factual basis or technical reasoning establishing that all

of the structures recited in claim 18 are inherent, i.e., must be present and necessarily follow from the operations recited in claim 1. A factual basis for the rejection should be provided, not merely an implication that claimed structure is disclosed. Claim 18 is not merely "an apparatus claim of claim 1, " but recite a particular structural arrangement not required by claim 1.

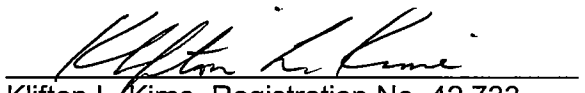
III. CONCLUSION

In view of the arguments submitted in the Appeal Brief and this Reply Brief, the Appellant respectfully submits that all the appealed claims in this application are patentable and requests that the Board of Patent Appeals and Interferences direct allowance of the rejected claims.

Appellant believes no further fees or petitions are required. However, if any such petitions or fees are necessary, please consider this a request therefor and authorization to charge Deposit Account No. 04-1415 accordingly.

Dated: November 16, 2007

Respectfully submitted,



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